PARALLEL SIMULATION OF FAULT AND FREEFAULT PSEUDO- BOOLEAN SCHEMES

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Запропоновано метод паралельного моделювання справних та несправних сучасних великих електронних приладів.

Digital devices manufactured by the MOS- and CMOS-technologies have some features of operation which complicate their simulation when being represented by the gate level models. The bidirectional character of signals presents no difficulties if healthy devices are under consideration but the fault simulation shows clearly the shortcommings of the conventional gate approach [1-3]. In [3] six shortages of the classical switching circuit theory are pointed out as applied to the analysis of modern VLSI MOS-circuits. The specific character of the MOS-circuit operation may be taken into consideration by simulation at the switching level [1-4] using various modification of Bryant's algorithm [5]. The aim of this work is to speed up the simulation procedures by constructing a parallel simulation algorithm at the switching level which is equivalent to Bryant's algorithm.

Going to the suggested method, note that the input data for the algorithm are, firstly, the description of the circuit having MOS- transistors differing in their high and low resistances, and the nodes characterized by high and low capacitance. For convenience this description is supposed to be equivalent to those in the "esim" language [4]. Secondly, the sequence of input signals is specified. The algorithm fields the signal values at each node of the device as responses to given input actions.

Let {*Z* (*C0*, *C1*), *CX*, (*SC0*, *SC1*), *SCX*, (*W0*, *W1*), *WX*, (*D0*, *D1*), *DX*} be the simplest signal set needed for *n*-MOS-circuit simulation which is ordered in reference to ≤. We use ordinary notations *D*, *W*, *SC* and *C* to describe the forces (controlled, weak, supercharged, and charged) and notation *0*, *1*, *X* to describe the node state [4]. So, for any signal *S* = *(H, G)*, where *H(G)* is the force value (state value). A particular place is occupied by the signal Z = (Z_H, Z_G), which is taken as node disconnection.

The signal value at node *v* in the MOS-circuit may be determined as the magnitude of the "strongest" signal among all signals caming to it by all acyclic paths passing through the conducting transistors from the device input nodes and the nodes where the capacity existed initially. There is a simple iterative technique for calculating the node response to the input actions for this rather complicated definition. Let the signal value at *u*(val(*u*)) be $S_u = (H_u, G_u)$. For each node *v* a new signal value $S^{(i)}$ is calculated in compliance with joining the previous value *v* and function values F_{uv}(val(*u*)) associated with the transistor between nodes *u* and *v* for all neighbours *u* of node *v* [4]. The calculations continue until $S^{(i+1)}$ is equal to $S^{(i)}$. Denote F_{uv} (val(*u*)) as *f* (*T*, *R*, H_u, G_u), where *u* is the node connected directly to *v* through a transistor of the *T* type which has the value *R* at its gate. The function *f* of the signal transformation when the signal is passing through the transistor will be considered later. These iterative calculations give wrong results for some complex circuits. Bryant's algorithm modifies the calculations performed by this calculation scheme, which is a ground for a so-called simple algorithm using the distributive transistor functions *f*. At first we consider the simple algorithm with the distributive transistor transformation functions and then proceed to Bryant's parallel algorithm.

Recall the transformation rules for a signal passing through transistors [2, 4]. First consider the circuits consisting of the *n*-MOS-transistors only. The switching-type *n*-MOS-transistor will be denoted as *T* = 1, while the load-type transistor (put instead of resistor in the MOS-circuits) *T* = 0. Denoting the transistor gate value by *R*, assume that *R* = 0 for the cut-off transistor and *R* = 1 for the conducting transistor. The first rule states that for the cut-off transistor, its source and drain have no effect on each other, i. e. are disconnected, and *f* (*T*, *R*, *H*, *G*) = *Z* at *R* = 0, *T* =1. It follows from the second rule that *f* (*T*, *R*, *H*, *G*) = (*H*, *G*) at *T* = 1 and *R* =1 which means full signal transition through the conducting switching transistor. The third rule defines the

conducting load transistor operation ($T = 0$). It may be written in the form $f(T, R, H, G) = (W, G)$ at $H = D$ or as $f(T, R, H, G) = (H, G)$, otherwise. Extending the transformation rules for signals passing through transistors [4], we can define the transformation function f for the signal $S = (H, G)$ passing through the T type transistor with the state signal value R at the gate:

$$f(T,R,H,G) = \begin{cases} Z \text{ at } T=1 \text{ and } R=0; \\ (H,G) \text{ at } T=1 \text{ and } R=1; \\ (H,G) \text{ at } T=0 \text{ and } H<D; \\ (W,G) \text{ at } T=0 \text{ and } H=D. \end{cases}$$

Now represent f by the totality of Boolean functions which may be evaluated in parallel for the simple algorithm and Bryant's algorithm. The forms of these functions depend on the force and state value coding. Since the main memory capacity is occupied by the link description, the saving of memory hardly depends at all on the coding type of the force signal or node state. So, in order to raise the simulation speed we assume the following signal coding: Z = (Z_h, Z_g), where Z_h = (0, 0, 0, 0) and Z_g= (0, 0, 0), D = (1, 0, 0, 0), W = (0, 1, 0, 0), SC = (0, 0, 1, 0), C = (0, 0, 0, 1), X = (1, 0, 0), 1= (0, 1, 0) and 0 = (0, 0, 1). Let $F = f(T, R, H, G)$, then for the bit components $F = (FH_1, FH_2, FH_3, FH_4, FG_1, FG_2, FG_3)$ for the chosen coding we obtain the following expressions, with the assumption that $R = (R_1, R_2, R_3)$, $H = (H_1, H_2, H_3, H_4)$ and $G = (G_1, G_2, G_3)$. For the node state values

$$FG_1 = G_1(\bar{T} \vee TR_2);\ FG_2 = G_2(\bar{T} \vee TR_2);$$

$$FG_3 = G_3(\bar{T} \vee TR_2); \qquad (1)$$

while for the force values

$$FH_1 = H_1TR_2; \quad FH_2 = H_2(TR_2 \vee \bar{T}\bar{H}_1) \vee \bar{T}\bar{H}_1;$$

$$FH_3 = H_3(TR_2 \vee \bar{T}\bar{H}_1); \quad FH_4 = H_4(TR_2 \vee \bar{T}\bar{H}_1). \qquad (2)$$

The simulation of the MOS- and C-MOS-structures poses the need introduce the p-MOS-transistor, which implies certain complication of the equation for the transformation function f, because if a large number of transistors are described, bit variables T_1, T_2 used for their coding are needed. Let for the load transistor T_1 = 0 (for T_2 -- indifferently); for the n-MOS-transistor we have $T_1 = 1$, $T_2 = 1$, and for the p-MOS-transistor $T_1 = 1$, $T_2 = 0$. Taking into account that the p-MOS-transistor, in the view of the logics, operates as a n-MOS-transistor with the inverse gate value, we get the equations similar to (1) and (2) :

$$FG_1 = G_1T_1K \vee G_1\bar{T}_1;$$

$$FG_2 = G_2T_1K \vee G_2\bar{T}_1;$$

$$FG_3 = G_3T_1K \vee G_3\bar{T}_1;$$

$$FH_1 = T_1H_1K;$$

$$FH_2 = T_1H_2K \vee \bar{T}_1H_2H_1 \vee T_1\bar{H}_1;$$

$$FH_3 = T_1H_3K \vee \bar{T}_1H_3\bar{H}_1;$$

$$FH_4 = T_1H_4K \vee \bar{T}_1H_4\bar{H}_1,$$

where $\oplus$ is the "exclusive-OR" operation and $K = R_2 \oplus \overline{T_2}$ For $T_2 = 1$ (only n-MOS-transistors) they pass to (1) and (2).

The types of MOS-circuit fault are depicted in figure 9.5 [6]. The simulation of a circuit with this fault is the simulation with a corresponding structure data.

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